Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	8	processors (ALU or (arithmetic adj logic)) (instruction adj process$4) (processor adj port$1) communication ratio	US-PGPUB; USPAT; USOCR; IBM_TDB	AND	OFF	2005/12/15 10:17
S2	1	processors (ALU or (arithmetic adj logic)) (instruction adj process$4) port$1 communication ratio DCC DCP	US-PGPUB; USPAT; USOCR; IBM_TDB	AND	OFF	2005/12/15 10:19
S3	162	processors (ALU or (arithmetic adj logic)) (instruction adj process$4) port$1 communication ratio	US-PGPUB; USPAT; USOCR; IBM_TDB	AND	OFF	2005/12/15 10:23
S4	133	processors (ALU or (arithmetic adj logic)) (instruction adj process$4) port$1 communication ratio config$6	US-PGPUB; USPAT; USOCR; IBM_TDB	AND	OFF	2005/12/15 10:23
S5	35	processors (ALU or (arithmetic adj logic)) (instruction adj process$4) port$1 communication ratio configurable	US-PGPUB; USPAT; USOCR; IBM_TDB	AND	OFF	2005/12/15 10:26
S6	27	processors (ALU or (arithmetic adj logic)) (instruction adj process$4) port$1 communication ratio configurable crossbar (IC or (integrated adj circuit$2)) register$2	US-PGPUB; USPAT; USOCR; IBM_TDB	AND	OFF	2005/12/15 10:26
S7	1	processors (ALU or (arithmetic adj logic)) (instruction adj process$4) port$1 communication ratio configurable crossbar (IC or (integrated adj circuit$2)) register$2 synchronous (power adj consumption)	US-PGPUB; USPAT; USOCR; IBM_TDB	AND	OFF	2005/12/15 10:27
S8	27	processors (ALU or (arithmetic adj logic)) (instruction adj process$4) port$1 communication ratio configurable crossbar (IC or (integrated adj circuit$2)) register$2 synchronous power	US-PGPUB; USPAT; USOCR; IBM_TDB	AND	OFF	2005/12/15 10:28
S9	2	processors (ALU or (arithmetic adj logic)) (instruction adj process$4) port$1 communication ratio configurable crossbar (IC or (integrated adj circuit$2)) register$2 synchronous power accumulator	US-PGPUB; USPAT; USOCR; IBM_TDB	AND	OFF	2005/12/15 10:28